

## REMARKS

The Applicant appreciates the time taken by the Examiner to review The Applicant's present application. This application has been carefully reviewed in light of the Examiner's comments, including the Office Action mailed May 18, 2007. The Applicant respectfully requests reconsideration and favorable action in this case.

### Summary of rejections and amendments

The Examiner rejected claims 1, 3, 4, 6-10, 12-16 and 18-19 under 35 U.S.C. §102, and claims 2, 5 and 17 under 35 U.S.C. 103. The Examiner objected to claim 11, but stated that the subject matter of the claim is allowable. The Applicant has amended claim 13. Claims 1-19 are therefore pending in the application.

### Rejections under 35 U.S.C. §102

Claims 1, 3, 4, 6-10, 12-16 and 18-19 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,799,234 ("Moon"). The Applicant respectfully traverses this rejection.

In order to anticipate a claim, the reference must teach every element of the claim. The elements must be arranged as required by the claim, and must be shown in as complete detail as is contained in the claim. M.P.E.P. 2131. The Applicant respectfully submits that the Moon reference fails to disclose the elements of the claims, as arranged in the claims, and in as much detail as is contained in the claims. Moon therefore fails to anticipate the claims.

The claims of the present application recite a system for synchronizing operation of a plurality of digital audio controller chips. Moon, on the other hand, discloses a system for assigning resources to a slave device inserted into a PCI backplane (see abstract.) While both the present system and the system described by Moon include master and slave devices, this is one of the few similarities between the systems, and Moon fails to disclose most of the limitations of the claims, as described in the following paragraphs.

Regarding claim 1, the Examiner states that Moon discloses a plurality of digital audio controller chips, citing Figure 1, items 10 (master) and 12 (slaves). In fact, these items are not digital audio controller chips. Item 10 is a network control card (col. 2, line 43) and items 12(1)-12(N) are stacked PC104+ cards (col. 2, line 44.) Moon therefore fails to disclose this limitation of claim 1.

While the Examiner correctly states that one of the devices of Moon (network control card 10) is a master and other devices (PC104+ cards 12) are slaves, and that each of these

devices is connected to a synchronization line (SYN,) the Examiner incorrectly states that each of the slaves is configured to detect a synchronization signal on this line and to begin synchronized operation in response to detecting the signal. Moon actually discloses that the signal transmitted on synchronization line SYN is a frame sync signal which is used to define the number of fixed-duration time slots in a frame (col. 2, lines 48-49; col. 3, lines 1-3 and 30-31.) Thus, Moon fails to disclose this limitation of claim 1 as well.

Because Moon fails to disclose the foregoing limitations of claim 1, Moon cannot anticipate claim 1. Accordingly, the Applicant requests that the rejection of claim 1 as anticipated by Moon be withdrawn. Further, since claims 3, 4, 6-10, 12-16 and 18-19 depend from claim 1 and include all the limitations of claim 1, Moon fails to anticipate these claims for the same reasons set forth above with respect to claim 1. The Applicant therefore respectfully requests that the rejection of these claims be withdrawn.

The Applicant points out that, although Moon fails to anticipate claims 1, 3, 4, 6-10, 12-16 and 18-19 for the reasons set forth above, claims 3, 4, 6-10, 12-16 and 18-19 include additional limitations that are not disclosed by Moon and are therefore further patentably distinguished from this reference.

Claim 3, for example, recites that the master (as well as the slaves) is configured to begin synchronized operation in response to detecting the synchronization signal on the synchronization line. The Examiner states that Moon discloses this limitation, citing col. 1, lines 20-21 ("master device initiates an information transfer.") Moon actually discloses that this information transfer is initiated on an SPI bus -- not a synchronization line. Further, there is no indication that the master detects any signal or begins synchronized operation in response to such a detected signal.

Claim 4 recites that the master is designated during an initialization process. The Examiner states that this is disclosed at col. 1, lines 20-21 of Moon. As noted above, this portion of Moon discloses that a master initiates an information transfer on an SPI bus -- there is no disclosure whatsoever regarding the designation of a master or the initialization of the system.

Claim 6 specifies that the synchronization signal comprises a transition from a passive state to an active state. The Examiner states that this is disclosed at col. 4, lines 18 and 26 ("switches 37 are closed" and "switches 37 are opened.") This portion of Moon clearly states that the opening and closing of switches 37 is responsive to a reset signal detected during a selected time slot, and not in response to the synchronization signal.

Claim 7 recites that the master is configured to repeat the synchronization signal transition at a fixed intervals. The Examiner states that this is disclosed at col. 3, line 1 of Moon ("the master controls the number of fixed duration.") Moon actually states at col. 1, lines 1-3 that "The master controls the number of fixed duration time slots in a frame by controlling the interval between assertion of the SYNC signal." The statement that the number of fixed duration time slots in a frame is controlled implies that the interval, and the number, is not fixed – if it were fixed, it would not need to be controlled. Moon therefore fails to disclose the recited limitation.

Claim 8 recites that the master is configured to maintain the active state for a fixed period after each transition. The Examiner states that Moon discloses this at col. 4, lines 5-6 ("The master asserts the chip select bit in the time slot assigned to the slave.") The Applicant points out that asserting the chip select bit (bit 2 in the time slot of Fig. 2) is entirely independent of the synchronization signal or whether the synchronization signal is maintained in an active state. Moon therefore fails to disclose the limitation of claim 8.

Claim 9 recites that each slave is configured to sample the synchronization line during the fixed period to determine whether the synchronization line is in an active state. The Examiner states that this limitation is disclosed by Moon at col. 4, lines 26-27. As noted above, this portion of Moon discloses the opening and closing of switches 37 in response to a reset signal which is detected during a selected time slot – it has nothing whatsoever to do with the slaves sampling the synchronization line. Thus, Moon fails to disclose the limitation of claim 9.

Claim 10 recites that each slave is configured to take multiple samples during the fixed period and to determine whether the synchronization line is in an active state based upon a majority of the multiple samples. The Examiner asserts that this is disclosed at col. 3, lines 57-60 of Moon. In fact, col. 3, lines 57-60 of Moon discloses the manner in which a slave attempts to assert the "assigned bit" in a time slot in order to be assigned to (associated with) that time slot. This has nothing to do with taking multiple samples of the synchronization line and determining the state of the synchronization line based on the samples. Moon therefore fails to disclose the limitation of claim 10.

Claim 12 recites that each slave is configured to filter samples of the synchronization line. The Examiner states that this is disclosed at col. 3, lines 65-67 of Moon. As pointed out above, this portion of Moon discloses that a slave attempts to assert the "assigned bit" in a time slot in order to be assigned to that time slot. This has nothing to do with filtering the samples of the synchronization line. Moon therefore fails to disclose the limitation of claim 12.

Claim 13 recites that the master is configured to transmit non-synchronization data to the slaves via the synchronization line. The Examiner asserts that this is disclosed in Fig. 1. In fact, the only use for the synchronization line (SYN) of Moon is to assert a SYNC signal at desired intervals to control the number of fixed-duration time slots in a frame. There is no disclosure whatsoever that any non-synchronization data is transmitted on Moon's synchronization line (SYN). Moon therefore fails to disclose the limitation recited in claim 13.

Claim 14 recites that the synchronization signal comprises a transition from a passive state to an active state, wherein the master is configured to maintain the active state for a fixed period, then transition from the active state to the passive state, then maintain the passive state for a fixed period, then transmit data. The Examiner asserts that this is disclosed in Fig. 1 and at col. 4, lines 18, 26 and col. 3, line 1. As pointed out above with respect to claims 6, 8 and 13, the cited portions of Moon do not disclose these limitations.

Claim 15 recites that each of the slaves is configured to determine whether an error has occurred and, in response to detecting an error, to cause the master to re-synchronize the slaves. The Examiner asserts that this is disclosed at col. 4, lines 9-13 ("If more than one slave selected the same assigned time slot, the master will detect the fact via a frame check sequence error on the SPU data. Having detected an error, the master issues a 'reset' signal to that time slot in the next frame.") As noted above, the reset signal and the events that occur following assertion of the reset signal are independent of the synchronization line and synchronization signal. Thus, Moon fails to disclose the limitation recited in claim 15.

Claim 16 recites a slave causing the master to re-synchronize by driving the synchronization line to the active state. The Examiner asserts that this is disclosed by Figs. 1 and 2. In fact, there is no disclosure whatsoever in Moon that the slaves can drive any signal on the synchronization line. Moon only discloses that the master controls assertion of the SNYC signal on the synchronization line (SYN). Moon therefore fails to disclose the limitation recited in claim 16.

Claim 18 recites that the master is configured to determine whether all of the slaves are ready to begin synchronized operation before generating the synchronization signal. The Examiner asserts that this is disclosed in Fig. 1 and at col. 1, lines 22-23. This portion of Moon, however, only discloses that a master can control a slave through a slave select (chip enable) line – there is no suggestion whatsoever that the master determines the slaves are ready to begin synchronized operation before generating a synchronization signal. Moon therefore fails to disclose the limitation of claim 18.

Claim 19 recites that each of the slaves drive the synchronization line to an active state until the slave is ready to begin synchronized operation, and the master determines that all of the slaves are ready to begin synchronized operation when the synchronization line is in a passive state. The Examiner asserts that this is disclosed in Fig. 1 and at col. 4, lines 18 and 26. As noted above, the slaves of Moon do not drive any signal on the synchronization line (SYN). Further, as also noted above, col. 4, lines 26-27 of Moon discloses the opening and closing of switches 37 in response to a reset signal which is detected during a selected time slot. This has nothing whatsoever to do with the slaves driving the synchronization line or the master detecting any particular state on the synchronization line. Consequently, Moon fails to disclose the limitation of claim 19.

For all of the foregoing reasons, Moon fails to anticipate claims 1, 3, 4, 6-10, 12-16 and 18-19. The Applicant therefore respectfully requests that the Examiner withdraw the rejections under 35 U.S.C. §102.

#### Rejections under 35 U.S.C. §103

Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Moon in view of U.S. Patent No. 5,822,779 ("Intrater"). The Applicant respectfully traverses this rejection.

The Examiner states that Moon teaches audio controller chips, but does not teach that the chips are PWM chips. The Examiner states that Intrater teaches PWM chips. The Applicant points out that, while Intrater does disclose PWM chips, neither Moon nor Intrater discloses audio controller chips. In fact, the word "audio" does not even appear in either of the references. The combined references therefore still fail to teach or suggest all of the limitations of the claim.

Further, even if one of the references disclosed anything relating to audio amplification, the Applicant respectfully submits that the Examiner has failed to show any motivation in the references or in the knowledge generally available to a person of ordinary skill in the art to combine the references. The Examiner merely states that the combination would have been obvious "since a PWM chip 'generates a square wave with a fixed frequency and a variable duty cycle.' " It is not at all clear to the Applicant how the ability to generate a square wave with a fixed frequency and a variable duty cycle would motivate a person of ordinary skill to modify the system of Moon as suggested.

Because the Examiner has failed to show that the cited references disclose all of the limitations of the claims or why a person of ordinary skill would be motivated to combine the references, the Applicant respectfully submits that the Examiner has failed to make a prima

facie case of obviousness as required by M.P.E.P. 2143.

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Moon in view of U.S. Patent No. 6,854,053 ("Burkhardt"). The Applicant respectfully traverses this rejection.

The Examiner states that Moon discloses master and slave chips, but that it does not disclose that the master and slaves have identical circuitry. The Examiner states that Burkhardt discloses master and slave chips that have identical circuitry, citing Fig. 1, items 12 and 14. While both master 12 and slaves 14 in Fig. 1 include a UART, the figure also clearly shows that master 12 includes a pull-up resistor connected to a power supply, which is not included in slaves 14. The master and slaves of Burkhardt therefore clearly do not have identical circuitry. Because this limitation, as well as the limitations discussed above with respect to claim 1, are not disclosed by the references, the Applicant respectfully submits that the Examiner has failed to make a prima facie case of obviousness of claim 5, as required by M.P.E.P. 2143.

Claim 17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Moon in view of U.S. Patent No. 6,639,956 ("Song"). The Applicant respectfully traverses this rejection.

The Examiner states that Moon discloses a system as recited in claim 1, but not the alignment and then staggering of the output phase of each controller. The Examiner states, however, that Song teaches chips intended for the alignment of the phase difference, citing col. 3, lines 42-43. The Examiner states that it would have been obvious to combine the references because the phases of the clock signals "need to be in sync" (citing col. 1, line 40.)

The Applicant notes that Song discloses the alignment of a local clock with a quarter clock. The Applicant also notes that neither the Examiner nor Song suggest that the phases of the clock signals (or any other signals) should be staggered as recited in claim 17. In fact, the phrase in Song cited by the Examiner – that the phases "need to be in sync" – teaches away from the staggering of the phases as recited in the claim. Because the references fail to teach or suggest the staggering of the phases (and in fact teach away from this,) the Applicant submits that the Examiner has failed to make a prima facie case of obviousness in accordance with M.P.E.P. 2143 with respect to claim 17.

For all of the foregoing reasons, the Applicant respectfully submits that the cited references are insufficient to support the rejections of claims 2, 5 and 17 under 35 U.S.C. §103. The Applicant therefore requests that the Examiner withdraw the rejections under 35 U.S.C. §103.

Allowable subject matter

The Examiner states that claim 11 is objected to as being dependent upon a rejected base claim, but that this claim would be allowable if rewritten in independent form, including the limitations of the base and intervening claims. The Applicant points out that, because the rejections of the claims from which claim 11 depend are believed to have been overcome as explained above, claim 11 is believed to be allowable. The Applicant therefore respectfully requests that the objection to this claim be withdrawn.

Conclusion

The Applicant has now made an earnest attempt to place this case in condition for allowance. Other than as explicitly set forth above, this reply does not include an acquiescence to statements, assertions, assumptions, conclusions, or any combination thereof in the Office Action.

For at least the foregoing reasons, the Applicant respectfully requests allowance of all claims pending in the application. The Examiner is invited to telephone the undersigned at the number listed below for prompt action in the event any issues remain.

If any extensions of time are necessary to prevent the above referenced application from becoming abandoned, the Applicant hereby petitions for such extensions. If any fees are inadvertently omitted, or if any additional fees are required, or if any amounts have been overpaid, please appropriately charge or credit those fees to Deposit Account No. 50-3085 of the Law Offices of Mark L. Berrier.

Respectfully submitted,



Mark L. Berrier  
Reg. No. 35,066

Dated: 6/29/07

Law Offices of Mark L. Berrier  
3811 Bee Caves Road, Suite 204  
Austin, Texas 78746  
telephone: 512.306.9200  
facsimile: 512.306.9952  
mberrier@texasIP.com